IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Aipperspach et al.	§	
	§	
Serial Number: 10/616,881	§	Group Art Unit: 2825
	§	
Filed: July 10, 2003	§	
	§	Examiner: Thuan V. Do
For: PULSE WIDTH LIMITED CHIP CLOCK DESIGN	§	
	§	

Commissioner of Patents and Trademarks
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APPLICANTS' APPEAL BRIEF

Applicants-inventors ("Applicants") and assignee International Business Machines Corporation respectfully submit the present brief in support of the patentability of the claims of the above-referenced application.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, of Armonk, New York, assignee of the interests in the invention from the named inventors.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 42-65 are pending. Of these, Claims 42 and 54 are independent Claims. Claims 1-41 have been withdrawn or canceled. Applicants appeal the Examiner's rejections of Claims 42-65 under 35 U.S.C. §101 and 35 U.S.C. §112, first paragraph.

IV. STATUS OF AMENDMENTS

The Claims stand as amended in the Request for Continued Examination (RCE) dated May 10, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

During chip manufacturing, circuit transistors are exposed to testing temperatures and voltages, which cause leakage currents to increase dramatically. *See* Application, Page 1, lines 17-19. Low frequency circuit tests, under extreme leakage conditions, make it very difficult to design dynamic logic circuits, because the dynamic logic circuits must be in the evaluation or testing phase for an extended period of time. *See* Application, Page 1, lines 20-24. A typical solution provides more "keeper" devices to maintain functionality under extreme test conditions. *See* Application, Page 1, line 28 to Page 2, line 1. Using an increased number of keeper devices, however, causes the nominal environment performance to suffer. *See* Application, Page 2, lines 1-2.

The present invention seeks, therefore, to reduce the effects of leakage currents on the dynamic parts of a chip design during low frequency testing. Specifically, the present invention limits a pulse width in the chip clock design of a circuit. *See* Application, Page 2, lines 8-9. The invention receives a clock signal with a pulse width and determines whether the received signal exceeds the maximum allowed pulse width—if it does, the clock pulse width is limited. *See* Application, Page 8, lines 28-29; Page 9, lines 5-8. The maximum pulse width is typically determined by the leakage current characteristics of the circuit under consideration. *See* Application, Page 5, lines 13-15. Figure 3 illustrates the particular embodiment under appeal herein.

The Claims embody the invention as follows:

Claim 42: A method of altering a duty cycle of a first clock signal in an integrated circuit having a plurality of switches, comprising:

receiving, by at least a first portion of the switches, the first clock signal, wherein the first clock signal has a first pulse width;

in response to the first clock signal transitioning from a first logical state to a second logical state at time t:

gating a second portion of the switches to transition a second clock signal to the second logical state at substantially time t;

at substantially time t, propagating a signal in the first logical state through a delay element, wherein the delay element has a propagation delay time t1;

in response to the propagation delay time t1 being less than the first pulse width of the first clock signal, at substantially the end of time t + t1, gating a third portion of the switches to transition the signal to the second logical state; and

in response to the signal transitioning to the second logical state, at substantially the end of time t + t1, transitioning the second clock signal to the first logical state; and

in response to the clock signal transitioning from the second logical state to the first logical state at time t2:

gating a fourth portion of the switches such that the second clock signal is in the first logical state at substantially time t2;

at substantially time t2, propagating the signal in the second logical state through the delay element; and

in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal, at substantially the end of time t2 + t1, gating a fifth portion of the switches such that the second clock signal does not transition to the second logical state at substantially the end of time t2 + t1.

Claim 54: An integrated circuit for altering a duty cycle of a first clock signal, the integrated circuit having a plurality of switches and comprising:

a first portion of the switches configured to receive the first clock signal, wherein the first clock signal has a first pulse width;

a second portion of the switches configured to transition a second clock signal to the second logical state at substantially time t, in response to the first clock signal transitioning from a first logical state to a second logical state at time t;

a delay element configured to propagate a signal in the first logical state at substantially time t, wherein the delay element has a propagation delay time t1;

a third portion of the switches configured to transition the signal to the second logical state, at substantially the end of time t + t1, in response to the propagation delay time t1 being less than the first pulse width of the first clock signal;

the second clock signal configured to transition to the first logical state in response to the signal transitioning to the second logical state at substantially the end of time t + t1;

a fourth portion of the switches configured to set the second clock signal in the first logical state at substantially time t2, in response to the clock signal transitioning from the second logical state to the first logical state at time t2;

the delay element further configured to propagate the signal in the second logical state at substantially time t2; and

a fifth portion of the switches configured to prevent the second clock signal from transitioning to the second logical state at substantially the end of time t2 + t1, in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal.

VI. GROUNDS OF REJECTION TO BE REVIEWED

Applicants filed a Specification supporting a number of elements including, "transitioning from a first logical state to a second logical state." Later, in a Request for Continued Examination, Applicants offered new Claims reciting, in part, "transitioning from a first logical state to a second logical state at time t." The Examiner rejected the new Claims under 35 U.S.C. §101 and §112, First Paragraph as new matter. Were the Examiner's rejections improper?

VII. ARGUMENT

A. Grouping of Claims

Claims 42 and 54 are independent. For purposes of this appeal, Applicants consider each of the independent Claims, and their respective dependent Claims, as separate groups. Thus, the groups of Claims are 42-53 and 54-65.

B. Summary of Pertinent Prosecution

Applicants filed the present application on July 10, 2003, with 19 Claims.

Applicants first amended the Claims in response to an Examiner telephone call on June 6, 2005, requesting election of Claims. In the Response, Applicants amended Claim 19 to depend from Claim 7 and added new Claims 20-21, obviating the restriction.

The Examiner mailed the first substantive action on June 28, 2005 ("First Action"), among other things, rejecting Claims 1-21 under 35 U.S.C. §102(e) as allegedly anticipated by Horan (US 6,704,908). The Examiner also rejected Claims 1-21 under 35 U.S.C. §103 in view of Horan and Hogan (US 5,535,337). The First Action also included a number of objections to Claim language as allegedly unclear.

Applicants' Response made corrective amendments to the specification, cancelled Claims 1-21, and entered new Claims 22-41.

The Examiner mailed the first final office action on December 5, 2005 ("First Final Action"). In the First Final Action, the Examiner again objected to a number of Claim elements and rejected Claims 22-41 under 35 U.S.C. §112, second paragraph, expressly relying on the many objections. The Examiner also relied on the objections as justification for not performing a search on the new Claims. The objections, therefore, formed the entirety of the First Final Action rejections.

Applicants filed a Request for Continued Examination on May 10, 2006 ("RCE"). In the RCE, Applicants cancelled Claims 22-41 and added new Claims 42-65, the Claims at issue in

this action. Claims 42 and 56 included the language, "at time t", "a propagation delay time t1", and "at time t2." Applicants also included a new Figure 3A, a timing diagram, about which Applicants stated, "Applicants submit that one skilled in the art could reproduce the added timing diagram and accompanying description solely from the invention as depicted in Figure 3." RCE, Page 13, lines 19-20.

The Examiner mailed the next substantive action on July 06, 2007 ("Second Action"). In the Second Action, the Examiner objected to Claims 42 and 54 and the new Figure as new matter. The Examiner also rejected Claims 42-65 under 35 U.S.C. §101 and 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement, based on "the timing such as at least t, t1, t1+1, t2, t2+t1 in the amended specification." Second Action, Page 2.

Applicants responded in a Response dated October 6, 2006, traversing the objections and rejections and arguing that the "new" timing diagram is not new matter because it could have been deduced by one of reasonable skill in the art. Further, Applicants argued that even if the timing diagram were new matter, which it is not, timing letters such as t, t1, etc., are so well known that their inclusion in a Claim cannot be objectionable new matter, and further that they are supported by the original Specification.

The Examiner mailed the second final action, the action under appeal herein, on November 22, 2006 ("Second Final Action"), maintaining the objections and rejections of Claims 42-65 under 35 U.S.C. §101 and 35 U.S.C. §112, first paragraph. This appeal followed.

C. Legal Requirements for a Section 101/112, First Paragraph Rejection

MPEP §2163 addresses new matter and adequate original disclosure considerations under 35 U.S.C. §112, first paragraph:

> The proscription against the introduction of new matter in a patent application (35 U.S.C. 132 and 251) serves to prevent an applicant from adding information that

> goes beyond the subject matter originally filed. *See In re Rasmussen*, 650 F.2d 1212, 1214, 211 USPQ 323, 326 (CCPA 1981) . . . While there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. . . The fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. *See, e.g., Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117.

MPEP §2163(I)(B). MPEP §2163 also provides general guidelines for examination under Section 112, first paragraph. In particular, there is a recommended procedure: "Office personnel should adhere to the following procedures when reviewing patent applications for compliance with the written description requirement of 35 U.S.C. 112, para. 1." MPEP §2163(II)(A).

In the first step, "Each claim must be separately analyzed and given its broadest reasonable interpretation in light of and consistent with the written description." MPEP §2163(II)(A)(1)(*citing In re Morris*, 127 F.3d 1048, 1053-54, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997)). During this step, "The entire claim must be considered, including the preamble language and the transitional phrase." MPEP §2163(II)(A)(1). Further, "The examiner should evaluate each claim to determine if sufficient structures, acts, or functions are recited to make clear the scope and meaning of the claim, including the weight to be given the preamble." MPEP §2163(II)(A)(1)(*citing Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620, 34 USPQ2d 1816, 1820 (Fed. Cir. 1995); *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir. 1989). Importantly, there is a clear standard, "The absence of definitions or details for well-established terms or procedures should not be the basis of a rejection under 35 U.S.C. 112, para. 1, for lack of adequate written description." MPEP §2163(II)(A)(1).

In the second step, the Examiner is to review the Specification, "Prior to determining whether the disclosure satisfies the written description requirement for the claimed subject matter, the examiner should review the claims and the entire specification, including the specific embodiments, figures, and sequence listings, to understand how applicant provides support for the various features of the claimed invention." MPEP §2163(II)(A)(2). In this step, "The analysis of whether the specification complies with the written description requirement calls for the examiner to compare the scope of the claim with the scope of the description to determine whether applicant has demonstrated possession of the claimed invention." MPEP §2163(II)(A)(2).

Importantly, "Such a review is conducted from the standpoint of one of skill in the art at the time the application was filed." MPEP §2163(II)(A)(2)(*citing Wang Labs. v. Toshiba Corp.*, 993 F.2d 858, 865, 26 USPQ2d 1767, 1774 (Fed. Cir. 1993)). In meeting this standard, "Generally, there is an inverse correlation between the level of skill and knowledge in the art and the specificity of disclosure necessary to satisfy the written description requirement" and "Information which is well known in the art need not be described in detail in the specification." MPEP §2163(II)(A)(2)(*citing Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1379-80, 231 USPQ 81, 90 (Fed. Cir. 1986)).

In the third and final step, the Examiner is to determine whether there is sufficient written description to inform a skilled artisan that the Applicants were "in possession of the claimed invention as a whole at the time the application was filed." MPEP §2163(II)(A)(3). In particular, regarding new matter, "To comply with the written description requirement of 35 U.S.C. 112, para. 1, . . . each claim limitation must be expressly, implicitly, or inherently supported in the originally filed disclosure." MPEP §2163(II)(A)(3)(b). Further, "When an explicit limitation in

a claim 'is not present in the written description whose benefit is sought it must be shown that a person of ordinary skill would have understood, at the time the patent application was filed, that the description requires that limitation.'" MPEP §2163(II)(A)(3)(b)(*quoting Hyatt v. Boone*, 146 F.3d 1348, 1353, 47 USPQ2d 1128, 1131 (Fed. Cir. 1998)).

D. Illustrative Claims of the Application

There are two Claim sets in the Pending Claims. Claim 42 recites:

42. A method of altering a duty cycle of a first clock signal in an integrated circuit having a plurality of switches, comprising:

receiving, by at least a first portion of the switches, the first clock signal, wherein the first clock signal has a first pulse width;

in response to the first clock signal transitioning from a first logical state to a second logical state at time t:

gating a second portion of the switches to transition a second clock signal to the second logical state at substantially time t;

at substantially time t, propagating a signal in the first logical state through a delay element, wherein the delay element has a propagation delay time t1;

in response to the propagation delay time t1 being less than the first pulse width of the first clock signal, at substantially the end of time t + t1, gating a third portion of the switches to transition the signal to the second logical state; and

in response to the signal transitioning to the second logical state, at substantially the end of time t + t1, transitioning the second clock signal to the first logical state; and

in response to the clock signal transitioning from the second logical state to the first logical state at time t2:

gating a fourth portion of the switches such that the second clock signal is in the first logical state at substantially time t2;

at substantially time t2, propagating the signal in the second logical state through the delay element; and

in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal, at substantially the end of time t2 + t1, gating a fifth portion of the switches such that the second clock signal does not transition to the second logical state at substantially the end of time t2 + t1.

Claim 54 recites:

54. An integrated circuit for altering a duty cycle of a first clock signal, the integrated circuit having a plurality of switches and comprising:

a first portion of the switches configured to receive the first clock signal, wherein the first clock signal has a first pulse width;

a second portion of the switches configured to transition a second clock signal to the second logical state at substantially time t, in response to the first clock signal transitioning from a first logical state to a second logical state at time t;

a delay element configured to propagate a signal in the first logical state at substantially time t, wherein the delay element has a propagation delay time t1;

a third portion of the switches configured to transition the signal to the second logical state, at substantially the end of time t + t1, in response to the propagation delay time t1 being less than the first pulse width of the first clock signal;

the second clock signal configured to transition to the first logical state in response to the signal transitioning to the second logical state at substantially the end of time t + t1;

a fourth portion of the switches configured to set the second clock signal in the first logical state at substantially time t2, in response to the clock signal transitioning from the second logical state to the first logical state at time t2;

the delay element further configured to propagate the signal in the second logical state at substantially time t2; and

a fifth portion of the switches configured to prevent the second clock signal from transitioning to the second logical state at substantially the end of time t2 + t1, in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal.

E. The Examiner's Rejections

The Examiner rejected Claims 52-65 under 35 U.S.C. §101 and 112, first paragraph as allegedly "failing to comply with the written description requirement." Second Final Action, Page 2. Specifically, "The claims 42, 54 contain new subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." Second Final Action, Page 2.

More particularly, the Examiner asserts that "The timing such as at least t, t1, t1+1, t2, t2+t1 in the amended specification dated 05/10/2006 and Figure 3A are the new matters to the current application." Second Final Action, Page 2. Applicants respectfully traverse these rejections in their entirety.

F. The Examiner's Rejections Were Procedurally and Factually in Error

1. The Timing Diagram is not New Matter

As described above, the Examiner's sole complaint regarding the pending Claims appears to be that the timing indications "t", "t1", etc. constitute new matter. Applicants respectfully submit that the use of the letter "t" to indicate timing indications, time periods, or the starting point of events is well-known to those skilled in the art. As such, the phrases, "transitioning from a first logical state to a second logical state at time t", "transition a second clock signal to the second logical state at substantially time t", and "wherein the delay element has a propagation delay time t1", as recited in Claims 42 and 54, for example, are crystal clear to one skilled in the relevant art. Accordingly, Applicants respectfully submit that the use of the timing indications "t", "t1", etc., clearly convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Moreover, the timing indications themselves are supported in the specification independent of the alleged "new matter" of Figure 3A. Figure 3 and the associated disclosure in the original Specification clearly supports the pending Claims as written. *See, e.g.,* Original Specification, at Page 8 ("Initially, the 'nclk_in' signal is high. Nodes a0-a20 are low, and the feedback signal 'fb' is low. As nclk_in goes to low, node a0 goes to high. After some delay, node a5 goes to high. Subsequently, nodes a10, a15, and a20 go to high sequentially. When node a20 goes high, node na20 goes low, turning on the first PMOS 302. This in turn drives node fb high. When node fb goes high, node a0 returns low again, forcing the output 'nclk_out' to go high."). In fact, in the RCE, Applicants expressly stated, "Applicants submit that one skilled in the art could reproduce the added timing diagram and accompanying description solely from the invention as depicted in Figure 3." RCE, Page 13. For at least this reason, the addition of the labels, "t", "t1", etc. to designate particular points in a method or timing references in a Specification-supported configuration cannot constitute "new matter." Further, as described in

more detail below, the timing indications, "t", "t1", etc., are well-enough known to those skilled in the art that adding them to the Specification-supported Claims does not constitute "new matter".

2. The Timing Indicia are Supported by the Original Specification

Applicants respectfully submit that the Examiner's Claim rejections in this case wholly fail to meet the standards required under Section 112, first paragraph, or Section 101. The impropriety of these rejections is best illustrated with respect to the MPEP-suggested framework.

First, regarding the Claims as a whole, Applicants respectfully submit that the timing diagrams and timing indicia in this case are clearly well-established terms and procedures. Especially in the context of the Claims as a whole, it is clear that Applicants were in position of the invention as now claimed. As such, the phrases, "transitioning from a first logical state to a second logical state at time t", "transition a second clock signal to the second logical state at substantially time t", and "wherein the delay element has a propagation delay time t1", as recited in Claims 42 and 54, for example, are crystal clear to one skilled in the relevant art. Even the use of the letter, "t" to indicate a timing signal is so well-known as to be almost a standard. As such, it is inappropriate for the Examiner to reject the Claims under Section 112, first paragraph based on the timing indicia. Accordingly, the Examiner's rejections fail under the first step of the appropriate examination standard. For this reason alone, the Examiner's rejections fail and should be withdrawn.

Next, regarding the second step, the Examiner is to review the Specification for Claim support, from the standpoint of one skilled in the art. Here, too, the Examiner's rejections also fail. Notwithstanding that the Examiner has not indicated any express determination of the appropriate skill level and knowledge in the art, Applicants submit that even at the most basic skill level, the timing indicia are clearly well within the reach of someone reasonably skilled in

the art. The use of timing indicia, such as the letter, "t", to indicate relative timings, clearly is "well known in the art" and therefore "need not be described in detail in the specification." *See* MPEP 2163(II)(A)(2). Further, timing indicia are so well-known that the inability to understand the term "transitioning from a first logical state to a second logical state at time t" could serve as a benchmark for those not "skilled in the art" at all. Accordingly, the Examiner's rejections also fail under the second step of the appropriate examination standard. For this reason alone, the Examiner's rejections fail and should be withdrawn.

Next, regarding the third step, analyzing whether the Claims as a whole and the Specification as read by one skilled in the art support the Claimed limitations, the Examiner's rejections also fail. Specifically, Applicants respectfully submit that the timing indicia are clearly supported by the description. That is, one skilled in the art would have understood that, for example, "transitioning from a first logical state to a second logical state" describes an event that must take place in some time period, given that events of any type in the art generally occur somewhere in space-time. Given that such an event occurs at a time, it is clear that naming that time, "t", serves to describe when the event occurs, so that other events may be described relative to that event, without also using confusing language.

For example, absent the time indicia, the label "t" for example, Claim 42 might read, in part, "transitioning a second clock signal to the second logical state at substantially the time of transitioning from a first logical state to the second logical state." Or worse, "in response to the propagation delay time of the delay element being less than the first pulse width of the first clock signal, at substantially the end of the sum of the time of transitioning from a first logical state to the second logical state and the propagation delay time of the delay element, gating a third portion of the switches to transition the signal to the second logical state."

Such repetition of the phrase, "transitioning from a first logical state to the second logical state" reduces clarity. However, substituting the appropriate time period referred to as "t" or "t+1" for example, illustrates how specious the Examiner's rejections truly are. Given that the claim limitations are clearly supported and readable, if less clear, with the substitutions, it is plain that the Applicants were "in possession of the claimed invention as a whole at the time the application was filed." Accordingly, the Examiner's rejections also fail under the third step of the appropriate examination standard. For this reason alone, the Examiner's rejections fail and should be withdrawn.

Moreover, the factual inquiry required under Section 112, first paragraph, does not relieve the Examiner of the burden to examine the Claims under the remaining patentability requirements. Specifically:

> The above only describes how to determine whether the written description requirement of 35 U.S.C. 112, para. 1, is satisfied. Regardless of the outcome of that determination, Office personnel must complete the patentability determination under all the relevant statutory provisions of title 35 of the U.S. Code.
>
> Once Office personnel have concluded analysis of the claimed invention under all the statutory provisions, including 35 U.S.C. 101, 112, 102, and 103, they should review all the proposed rejections and their bases to confirm their correctness. Only then should any rejection be imposed in an Office action. The Office action should clearly communicate the findings, conclusions, and reasons which support them.

MPEP 2163(III). In the present Application, the Examiner has also wholly failed to address patentability under 35 U.S.C. §102 or 103. Accordingly, Applicants submit that the Claims are therefore patentable in light of 35 U.S.C. §102 and 103. As Applicants have clearly demonstrated that the Examiner's only rejections fail, Applicants therefore respectfully submit

that Claims 42-65 are in condition for allowance. Applicants therefore respectfully request the Claims 42-65 be allowed.

Accordingly, Applicants respectfully submit that the Examiner's stated grounds are insufficient to maintain the Final Rejection. Applicants therefore respectfully request that the Final Rejections be withdrawn and that Claims 42-65 be allowed.

VIII. CLAIMS APPENDIX

See Attached.

IX. EVIDENCE APPENDIX

NONE.

X. RELATED PROCCEDINGS APPENDIX

NONE.

CONCLUSION

For the foregoing reasons, it is respectfully submitted that the Final Rejections of Claims 42-65 under 35 U.S.C. §§101, and 112, first paragraph, are improper and should be reversed. Applicants respectfully request that the rejections of Claims 42-65 be withdrawn and that Claims 42-65 be allowed.

Respectfully submitted,

Dated: April 23, 2007

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VIII – APPENDIX – CLAIMS ON APPEAL

42. (Previously Presented) A method of altering a duty cycle of a first clock signal in an integrated circuit having a plurality of switches, comprising:

receiving, by at least a first portion of the switches, the first clock signal, wherein the first clock signal has a first pulse width;

in response to the first clock signal transitioning from a first logical state to a second logical state at time t:

gating a second portion of the switches to transition a second clock signal to the second logical state at substantially time t;

at substantially time t, propagating a signal in the first logical state through a delay element, wherein the delay element has a propagation delay time t1;

in response to the propagation delay time t1 being less than the first pulse width of the first clock signal, at substantially the end of time t + t1, gating a third portion of the switches to transition the signal to the second logical state; and

in response to the signal transitioning to the second logical state, at substantially the end of time t + t1, transitioning the second clock signal to the first logical state; and

in response to the clock signal transitioning from the second logical state to the first logical state at time t2:

gating a fourth portion of the switches such that the second clock signal is in the first logical state at substantially time t2;

at substantially time t2, propagating the signal in the second logical state through the delay element; and

in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal, at substantially the end of time t2 + t1, gating a fifth portion of the switches such that the second clock signal does not transition to the second logical state at substantially the end of time t2 + t1.

43. (Previously Presented) The method of Claim 42, further comprising:

in response to the propagation delay time t1 being equal to or greater than the pulse width of the first clock signal, gating a sixth portion of the switches such that the second clock signal transitions in substantial accordance with the first clock signal, such that the duty cycle of the first clock signal is substantially identical to a duty cycle of the second clock signal.

44. (Previously Presented) The method of Claim 42, wherein the first portion of switches comprises four digital switches, wherein two digital switches are gated on and two digital switches are gated off in response to the first clock signal transitioning to the first logical state.

45. (Previously Presented) The method of Claim 42, wherein the delay element comprises at least two delay blocks coupled in series, wherein each delay block inverts the signal.

46. (Previously Presented) The method of Claim 45, wherein each delay block comprises at least a multiple of four NAND gates coupled in series.

47. (Previously Presented) The method of Claim 42, wherein the integrated circuit is one of a pulse limiting circuit or a processor.

48. (Previously Presented) The method of Claim 42, wherein the first logical state is a logical 1 and the second logical state is a logical 0.

49. (Previously Presented) The method of Claim 42, wherein the second portion of switches comprises:

a first digital switch, also in the first portion, coupled to an inverter and a second digital switch, and gated on in response to the first clock signal being in the second logical state; and

the second digital switch coupled to a logical 1 power supply and to the first digital switch, and gated on in response to a portion of the third portion of switches being gated off, wherein in response to the first digital switch and second digital switch being gated on, the logical 1 power supply drives the second clock signal to the second logical state.

50. (Previously Presented) The method of Claim 49, wherein the third portion of switches comprises:

a third digital switch coupled to the logical 1 power supply and a fourth digital switch, and gated by an inverse of the signal, wherein the third digital switch is gated on in response to the signal being in the first logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated on in response to the first clock signal being in the second logical state; and

a fifth digital switch coupled to logical 0 ground and an inverter, and gated by the fourth digital switch, wherein the fifth digital switch is gated on and transitions the signal to the second logical state in response to the third and fourth digital switches being gated on.

51. (Previously Presented) The method of Claim 42, wherein the step of transitioning the second clock signal to the first logical state comprises inverting the signal from the second logical state to the first logical state, thereby transitioning the second clock signal to the first logical state.

52. (Previously Presented) The method of Claim 42, wherein the fourth portion of switches comprises a digital switch, also in the first portion, wherein the digital switch is gated on in response to the first clock signal being in the first logical state, the digital switch being coupled to a logical 0 ground and an inverter such that when gated on, the digital switch drives the second clock signal to the first logical state.

53. (Previously Presented) The method of claim 50, wherein the fifth portion of switches comprises:

the third digital switch coupled to logical 1 voltage supply and gated by an inverse of the signal, wherein the third digital switch is gated off in response to the signal being in the second logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated off in response to the first clock signal being in the first logical state;

the fifth digital switch coupled to logical 0 ground and gated by the fourth digital switch, wherein the fifth digital switch is gated off in response to the fourth digital switch being gated off;

a sixth digital switch, also in the first portion, coupled to an inverter and gated by the first clock signal, wherein the sixth digital switch is gated on in response to the first clock signal being in the second logical state;

a seventh digital switch coupled to a logical 1 power supply and the sixth digital switch, and gated by the fourth digital switch, wherein the seventh digital switch is gated on in response to the fourth digital switch being gated off; and

wherein in response to the sixth and seventh digital switches being gated on, the sixth digital switch maintains the second clock signal at the first logical state.

54. (Previously Presented) An integrated circuit for altering a duty cycle of a first clock signal, the integrated circuit having a plurality of switches and comprising:

a first portion of the switches configured to receive the first clock signal, wherein the first clock signal has a first pulse width;

a second portion of the switches configured to transition a second clock signal to the second logical state at substantially time t, in response to the first clock signal transitioning from a first logical state to a second logical state at time t;

a delay element configured to propagate a signal in the first logical state at substantially time t, wherein the delay element has a propagation delay time t1;

a third portion of the switches configured to transition the signal to the second logical state, at substantially the end of time t + t1, in response to the propagation delay time t1 being less than the first pulse width of the first clock signal;

the second clock signal configured to transition to the first logical state in response to the signal transitioning to the second logical state at substantially the end of time t + t1;

a fourth portion of the switches configured to set the second clock signal in the first logical state at substantially time t2, in response to the clock signal transitioning from the second logical state to the first logical state at time t2;

the delay element further configured to propagate the signal in the second logical state at substantially time t2; and

a fifth portion of the switches configured to prevent the second clock signal from transitioning to the second logical state at substantially the end of time t2 + t1, in response to the propagation delay time t1 of the delay element being less than the first pulse width of the first clock signal.

55. (Previously Presented) The integrated circuit of Claim 54, further comprising:

a sixth portion of the switches configured to transition the second clock signal in substantial accordance with the first clock signal, such that the duty cycle of the first clock signal is substantially identical to a duty cycle of the second clock signal, in response to the propagation delay time t1 being equal to or greater than the pulse width of the first clock signal.

56. (Previously Presented) The integrated circuit of Claim 54, wherein the first portion of switches comprises four digital switches, wherein two digital switches are gated on and two

digital switches are gated off in response to the first clock signal transitioning to the first logical state.

57. (Previously Presented) The integrated circuit of Claim 54, wherein the delay element comprises at least two delay blocks coupled in series, wherein each delay block inverts the signal.

58. (Previously Presented) The integrated circuit of Claim 57, wherein each delay block comprises at least a multiple of four NAND gates coupled in series.

59. (Previously Presented) The integrated circuit of Claim 54, wherein the integrated circuit is one of a pulse limiting circuit or a processor.

60. (Previously Presented) The integrated circuit of Claim 54, wherein the first logical state is a logical 1 and the second logical state is a logical 0.

61. (Previously Presented) The integrated circuit of Claim 54, wherein the second portion of switches comprises:

a first digital switch, also in the first portion, coupled to an inverter and a second digital switch, and gated on in response to the first clock signal being in the second logical state; and

the second digital switch coupled to a logical 1 power supply and to the first digital switch, and gated on in response to a portion of the third portion of switches being gated off,

wherein in response to the first digital switch and second digital switch being gated on, the logical 1 power supply drives the second clock signal to the second logical state.

62. (Previously Presented) The integrated circuit of Claim 61, wherein the third portion of switches comprises:

a third digital switch coupled to the logical 1 power supply and a fourth digital switch, and gated by an inverse of the signal, wherein the third digital switch is gated on in response to the signal being in the first logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated on in response to the first clock signal being in the second logical state; and

a fifth digital switch coupled to logical 0 ground and an inverter, and gated by the fourth digital switch, wherein the fifth digital switch is gated on and transitions the signal to the second logical state in response to the third and fourth digital switches being gated on.

63. (Previously Presented) The integrated circuit of Claim 54, wherein transitioning the second clock signal to the first logical state comprises inverting the signal from the second logical state to the first logical state, thereby transitioning the second clock signal to the first logical state.

64. (Previously Presented) The integrated circuit of Claim 54, wherein the fourth portion of switches comprises a digital switch, also in the first portion, wherein the digital switch is gated on in response to the first clock signal being in the first logical state, the digital switch being

coupled to a logical 0 ground and an inverter such that when gated on, the digital switch drives the second clock signal to the first logical state.

65. (Previously Presented) The integrated circuit of claim 64, wherein the fifth portion of switches comprises:

the third digital switch coupled to logical 1 voltage supply and gated by an inverse of the signal, wherein the third digital switch is gated off in response to the signal being in the second logical state;

the fourth digital switch coupled to the third digital switch and gated by the first clock signal, wherein the fourth digital switch is gated off in response to the first clock signal being in the first logical state;

the fifth digital switch coupled to logical 0 ground and gated by the fourth digital switch, wherein the fifth digital switch is gated off in response to the fourth digital switch being gated off;

a sixth digital switch, also in the first portion, coupled to an inverter and gated by the first clock signal, wherein the sixth digital switch is gated on in response to the first clock signal being in the second logical state;

a seventh digital switch coupled to a logical 1 power supply and the sixth digital switch, and gated by the fourth digital switch, wherein the seventh digital switch is gated on in response to the fourth digital switch being gated off; and

wherein in response to the sixth and seventh digital switches being gated on, the sixth digital switch maintains the second clock signal at the first logical state.